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10/803,646	03/18/2004	Daniel Morgan Crowell	ROC920030393US1	5349

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EXAMINER	
TRUONG, LOAN	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/803,646	CROWELL ET AL.	
	Examiner	Art Unit	
	LOAN TRUONG	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/18/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 19* is/are allowed.

6)☒ Claim(s) *1-8, 10-18 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

Claims 9 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

1. Claims 22-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

In regards to claims 22-23, applicants claims a program product and a signal bearing medium, which does not fall within the statutory category for patentably and therefore is non-statutory. See MPEP § 2106. Examiner suggests that the program be embodied in a computer readable medium being executed by a processing system and the signal bearing medium be further specified to one of the statutory category.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-8, 10-18 and 20-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Cepulis et al. (US 6,496,945).

In regard to claim 1, Cepulis et al. disclosed a method of booting a computer, the method comprising:

initiating a boot operation (*POST, col. 2 lines 23-30)*;

detecting a failure after initiation of and during performance of the boot operation (*During execution of POST routines various devices are tested to ascertain whether each device is working properly, col. 2 lines 23-30)*;

initiating a targeted diagnostic operation on at least one hardware device in the computer in response to detecting the failure (*read failed device log from NVRAM and tag logical resources that correspond to failed physical device as not available, fig. 2, 204, 212)*; and completing the boot operation after initiating the diagnostic operation (*continue with initialization, fig. 2, 216).*

In regard to claim 2, Cepulis et al. disclosed the method of claim 1, wherein the boot operation comprises a fast boot operation (*during boot-up, the BIOS code reads the failed device log to determine which logical devices were previously reported as failed to create a logical resource map, col. 2 lines 57-63).*

It is inherent that by utilizing the FDL stored in the NVRAM for initialization, it would equate to a faster boot operation as compared to doing the diagnostic within each boot operation.

In regard to claim 3, Cepulis et al. disclosed the method of claim 1, wherein the failure is associated with a failed hardware device (*POST routines to test each device, col. 2 lines 23-30)*, and wherein detecting the failure is performed prior to performing a diagnostic operation on the failed hardware device (*read failed device log from NVRAM and tag logical resources that correspond to failed physical device as not available, fig. 2, 204, 212).*

In regard to claim 4, Cepulis et al. disclosed the method of claim 1, wherein initiating the targeted diagnostic operation identifies a failed hardware device, the method further comprising isolating the failed hardware device responsive to the targeted diagnostic operation (*continue with initialization and only report available logical devices to O/S, fig. 2, 216).*

In regard to claim 5, Cepulis et al. disclosed the method of claim 4, wherein isolating the failed hardware device comprises deconfiguring the failed hardware device (*continue with initialization and only report available logical devices to O/S, fig. 2, 216).*

In regard to claim 6, Cepulis et al. disclosed the method of claim 4, further comprising reconfiguring the computer to account for isolating the failed hardware device in response to the targeted diagnostic operation (*continue with initialization and only report available logical*

devices to O/S, fig. 2, 216).

In regard to claim 7, Cepulis et al. disclosed the method of claim 1, wherein the targeted diagnostic operation is initiated in response to a detected failure only for those hardware devices that are potential sources of the detected failure (*read failed device log from NVRAM and tag logical resources that correspond to failed physical device as not available, fig. 2, 204, 212).*

In regard to claim 8, Cepulis et al. disclosed the method of claim 1, further comprising logging an error detected by the targeted diagnostic operation (*failed device log from NVRAM, fig. 2, 204).*

In regard to claim 10, Cepulis et al. disclosed the method of claim 1, wherein detecting the failure, initiating the targeted diagnostic operation (*read failed device log from NVRAM and tag logical resources that correspond to failed physical device as not available, fig. 2, 204, 212)* and completing the boot operation are performed without user intervention (*continue with initialization, fig. 2, 216).*

In regard to claim 11, Cepulis et al. disclosed an apparatus, comprising:

at least one processor (*CPU 0-n, fig. 1, 102)*; and

program code (*BIOS code, fig. 1, 122)* configured to be executed by the at least one processor to initiate a boot operation (*one of the CPU is designated as the "boot strap" processor, col. 7 lines 1-9)*, detect a failure after initiation of and during performance of the boot

operation (*during execution of POST routines various devices are tested to ascertain whether each device is working properly, col. 2 lines 23-30)*, initiate a targeted diagnostic operation on at least one hardware device in response to detecting the failure (*read failed device log from NVRAM and tag logical resources that correspond to failed physical device as not available, fig. 2, 204, 212)*, and complete the boot operation after initiating the targeted diagnostic operation (*continue with initialization, fig. 2, 216).*

In regard to claim 12, Cepulis et al. disclosed the apparatus of claim 11, wherein the boot operation comprises a fast boot operation (*during boot-up, the BIOS code reads the failed device log to determine which logical devices were previously reported as failed to create a logical resource map, col. 2 lines 57-63).*

It is inherent that by utilizing the FDL stored in the NVRAM for initialization, it would equate to a faster boot operation as compared to doing the diagnostic within each boot operation.

In regard to claim 13, Cepulis et al. disclosed the apparatus of claim 11, wherein the failure is associated with a failed hardware device (, and wherein the program code (*BIOS code, fig. 1, 122)* is configured to detect the failure (*FDL of NVRAM, fig. 2, 132)* prior to performing a diagnostic operation on the failed hardware device (*during execution of POST routines various devices are tested to ascertain whether each device is working properly, col. 2 lines 23-30).*

In regard to claim 14, Cepulis et al. disclosed the apparatus of claim 11, wherein the program code (*BIOS code, fig. 1, 122)* is configured to identify a failed hardware device in response to initiating the targeted diagnostic operation (*FDL of NVRAM, fig. 2, 132)*, and wherein the program code (*BIOS code, fig. 1, 122)* is further configured to isolate the failed hardware device responsive to the targeted diagnostic operation (*continue with initialization and only report available logical devices to O/S, fig. 2, 216).*

In regard to claim 15, Cepulis et al disclosed the apparatus of claim 14, wherein the program code is configured to isolate the failed hardware device by deconfiguring the failed hardware device (*continue with initialization and only report available logical devices to O/S, fig. 2, 216).*

In regard to claim 16, Cepulis et al. disclosed the apparatus of claim 14, wherein the program code is further configured to reconfigure the apparatus to account for isolating the failed hardware device in response to the targeted diagnostic operation (*continue with initialization and only report available logical devices to O/S, fig. 2, 216).*

In regard to claim 17, Cepulis et al. disclosed the apparatus of claim 11, wherein the targeted diagnostic operation is initiated in response to a detected failure only for those hardware devices that are potential sources of the detected failure (*read failed device log from NVRAM and tag logical resources that correspond to failed physical device as not available, fig. 2, 204, 212).*

In regard to claim 18, Cepulis et al. disclosed the apparatus of claim 11, wherein the program code is further configured to log an error detected by the targeted diagnostic operation *(failed device log from NVRAM, fig. 2, 204).*

In regard to claim 20, Cepulis et al. disclosed the apparatus of claim 11, wherein the program code is configured to detect the failure, initiate the targeted diagnostic operation (*read failed device log from NVRAM and tag logical resources that correspond to failed physical device as not available, fig. 2, 204, 212)* and complete the boot operation without user intervention (*continue with initialization, fig. 2, 216).*

In regard to claim 21, Cepulis et al. disclosed the apparatus of claim 20, wherein the at least one processor includes a service processor, wherein at least a portion of the program code (*BIOS code, fig. 1, 122)* is configured to be executed by the service processor (*one of the CPU is designated as the "boot strap" processor, col. 7 lines 1-9).*

In regard to claim 22, Cepulis et al. disclosed a program product, comprising:

program code (*BIOS code, fig. 1, 122)* configured to initiate a boot operation on a computer (*one of the CPU is designated as the "boot strap" processor, col. 7 lines 1-9)*, detect a failure after initiation of and during performance of the boot operation (*During execution of POST routines various devices are tested to ascertain whether each device is working properly, col. 2 lines 23-30)*, initiate a targeted diagnostic operation on at least one hardware device in the computer in response to detecting the failure (*read failed device log from NVRAM and tag*

logical resources that correspond to failed physical device as not available, fig. 2, 204, 212), and complete the boot operation after initiating the targeted diagnostic operation (*continue with initialization, fig. 2, 216)*; and

a computer readable signal bearing medium bearing the program code (*ISA bus, fig. 2, 120)*.

In regard to claim 23, Cepulis et al. disclosed the program product of claim 22, wherein the computer readable signal bearing medium (*ISA bus, fig. 2, 120)* includes at least one of a transmission medium (*ISA bus, fig. 2, 120)* and a recordable medium (*NVRAM, fig. 2, 132)*.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loan Truong whose telephone number is (571) 272-2572. The examiner can normally be reached on M-F from 8am-4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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